REMARKS/ARGUMENTS

Prior to this Amendment, claims 1-3, 5, 7, 10, 12, and 17-22 were pending in the application.

Claim 1 is amended to clarify that an intermediary mass storage controller, such as a disk controller, is not included in the computing system with a bus controller being configured to conduct mass storage transactions. Support is found at least in Figure 2 and corresponding text, and hence, no new matter is added by the amendment.

New independent claim 32 is added to further protect features of the invention. Support is found at least in the original figures, such as Figure 2 and supporting portions of the specification.

After entry of the Amendment, claims 1-3, 5, 7, 10, 12, 17-22, and 32 remain for consideration by the Examiner.

Rejections under 35 U.S.C. §102

In the Office Action mailed August 31, 2005, claims 1, 5, 7, and 10 were rejected under 35 U.S.C. §102(b) based upon "Operating Systems, Design and Implementation ("Tanenbaum"). This rejection is respectfully traversed based on the following remarks.

As amended, claim 1 calls for a bus controller having a memory interface to data memory and to a mass storage interface "without an intermediary mass storage controller." The claimed system provides a significant improvement over prior art systems, such as that shown in Figure 1 of Applicant's specification, because of the removal of the mass storage controller 103 and its additional interfaces and other complexities. Such an improvement is shown by way of example in the system of Figure 2, which shows a bus controller with an interface to both data memory and to a mass storage interface without a mass storage controller.

In direct contrast, Tanenbaum is cited in the Office Action as teaching the bus controller of claim 1 with its "Disk controller with DMA" at page 3 of the Office Action. However, this disk controller is a mass storage controller as shown in Applicant's Figure

1, and Tanenbaum fails to show a bus controller associated with its CPU that can "conduct mass storage transactions" as called for in claim 1. Claim 1 is not, therefore, anticipated by Tanenbaum because at least the bus controller configured as required by the language of claim 1 is not shown or even suggested by Tanenbaum.

Further as discussed in the prior Amendment, claim 1 calls for a data memory coupled to and shared by both the processor and the mass storage device. The disk controller in Tanenbaum is not a mass storage device as called for in claim 1 but is instead an interface to a mass storage device labeled "disk" in Tanenbaum, i.e., is a mass storage controller with such an interface. However, even if the disk controller were to be integrated with the disk in Tanenbaum, the reference shows a disk controller having memory (labeled "buffers") that is separate from and independent of the block labeled memory. Tanenbaum does not fairly suggest that the disk controller buffers could be implemented in the memory, or that the memory could be implemented by the disk controller buffers, so as to provide a data memory coupled to and shared by both the processor and the mass storage device as called for in claim 1. For these additional reasons, claim 1 is allowable over the Tanenbaum reference.

Claims 5, 7, and 10 depend from claim 1 and are allowable for at least the same reasons as claim 1.

Further, in the August 31, 2005 Office Action, claims 1-3 and 21 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. Publ. No. 2003/0037198 ("Hunsaker"). This rejection is traversed based on the following remarks.

Hunsaker, like Tanenbaum, fails to teach the bus controller as called for in claim 1. The Office Action cites the ICH 150 of Hunsaker for teaching the bus controller of claim 1, but from a review of paragraphs [0019] and [0020] it is apparent that the ICH 150 is similar to the prior art bus controller 101 shown in Applicant's Figure 1 and not the bus controller of claim 1 (such as controller 201 of Applicant's Figure 2). Specifically, the ICH 150 is described as including a PCI bus interface and USB interfaces (as is the case with controller 101) to enable it to interface with interfaces of a mass storage controller, such as controller 103 of Figure 1. There is no description in

these paragraphs regarding ICH 150 that there is no mass storage controller provided in mass storage device 170 or that the ICH 150 it is configured to "conduct mass storage transactions between the data memory and the mass storage device." Hence, Hunsaker fails to teach the bus controller of claim 1 and does not anticipate the system of claim 1.

Further, as discussed in prior responses, Hunsaker shows a system in which the mass storage devices couple to the processor through an intermediate mechanism, the ICH 150. Neither the memory controller hub 130 or the ICH 150 have both an interface coupled to the data memory and a mass storage interface. It is not proper to treat the combination of MCH 130 and ICH 150 as a single device as it is core to the Hunsaker device that these elements be implemented as separate devices. As such, they introduce a mandatory interface between the devices that must be traversed by mass storage transactions. The invention of claim 1 eliminates this need for excessive interface traversal and therefore provides an improvement over the architecture of Hunsaker. Claims 2, 3, and 21 depend from claim 1 and are believed allowable as depending from an allowable base claim.

Yet further, claims 1, 12, 13, and 20 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. No. 6,601,126 ("Zaidi"). This rejection is traversed based on the following remarks.

As discussed in prior responses, in Fig. 38, Zaidi shows a computer architecture in which a bridge device, not a data/control. bus, couples various components. Hence, there is no controller coupled to the CPU bus as called for in claim 1, nor is there a data memory coupled to the processor as called for in claim 1. Instead, the DRAM is coupled to the memory bus (m-bus). Moreover, Zaidi does not teach that the bridge is capable of conduct mass storage transactions between the data memory and the mass storage device. Similarly, Zaidi does not teach that the MAC is capable of conduct mass storage transactions between the data memory and the mass storage device. For these reasons, claim 1 is not anticipated by Zaidi. Claims 12, 13 and 20, which depend from claim 1, are allowable over Zaidi for at least the same reasons as claim 1.

Also, the Office Action rejected claims 1, 14, and 20 under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. No. 6,128,669 ("Moriarty"). This rejection is traversed based on the following remarks.

In Fig. 1 Moriarty et al. show a computer architecture in which a bridge device 106 is required for mass storage transactions. Hence, Moriarty does not show a controller that includes both a mass storage interface and an interface to the data memory as called for in claim 1. Instead, memory controller 108 enables memory transactions between the processor and the memory and a separate bridge 106 enables mass storage transactions. Hence, mass storage transactions must traverse multiple interfaces including the SCSI controller, PCI Bus, and Host bus. This multiple bus traversal is minimized in the invention of claim 1. Claims 14 and 20, which depend from claim 1, are allowable over Moriarty for at least the same reasons as claim 1.

Claims 1, 13-16, and 20-22 were rejected under 35 U.S.C. §102(e) based upon U.S. Pat. Publ, No. 2003/0181205 ("Yiu"). This rejection is respectfully traversed because Yiu in Figure 3 and elsewhere fails to show the bus controller of claim 1 that is provided for interfacing with mass storage devices without a mass storage controller. In Paragraph [0034] the processor 31 is described as having some similar features as the bus controller of prior art system in Applicant's Figure 1 for interfacing with a mass storage controller of the storage 34 of Yiu. Hence, the bus controller that interfaces with a mass storage device without an intermediary mass storage controller is not shown or suggested by Yiu.

Further, as discussed in the prior amendments, the Examiner relies on Fig. 3 of Yiu et al. to show the specific architecture called for in claim 1. However, Yiu states in paragraph 32 that "...FIG. 3 is not intended to represent any one specific physical arrangement." Accordingly, Fig. 3 does not show a real computer architecture and cannot be relied on to show or suggest the limitations of claims 1, 13-6, and 20-22. Specifically, one cannot, even today, obtain a mass storage device 34 such as a magnetic disk or CDROM that interfaces directly to the same bus as RAM and a processor. Yiu does not identify any such devices and so fails to provide an enabling disclosure of such a system. In contrast, the present invention teaches how to build

such a system including such a mass storage device by providing a controller having a memory interface and a mass storage interface. The list of various devices that appears in paragraph 34 of Yiu et al. describe types of processors and does not disclose a single device that would show or suggest the controller of claim 1. Claims 13-16 and 20-22 that depend from claim 1 are distinct over Yiu for at least the same reasons as claim 1.

Still further, claims 1 and 19 were rejected in the Office Action under 35 U.S.C. §102(e) based upon U.S. Pat. Appl. Publ. No. 2002/0144121 ("Ellison"). This rejection is respectfully traversed as claim 1 is believed allowable over Ellison at least for the reasons provided for allowing claim 1 over Hunsaker as Ellison's Fig. 1C and Hunsaker's Figure 1 provide similar teaching, and hence, have similar failings relative to claim 1.

Further, as discussed in prior amendments, Ellison shows a system in which the mass storage devices couple to the processor through an intermediate mechanism, the ICH 150. Neither the memory controller hub 130 or the ICH 150 have both an interface coupled to the data memory and a mass storage interface. It is not proper to treat the combination of MCH 130 and ICH 150 as a single device as it is core to the Ellison device that these elements be implemented as separate devices. As such, they introduce a mandatory interface between the devices that must be traversed by mass storage transactions. The invention of claims 1 and 19 call for a single controller having a memory interface and a mass storage interface that eliminates this need for excessive interface traversal and therefore provides an improvement over the architecture of Ellison.

Additionally, claims 17 and 18, which depend from claim 1, was rejected under 35 U.S.C. §102(e) based upon U.S. Pat. No. 6,493,656 ("Houston"). This rejection is respectfully traversed because the bus controller of claim 1 is not shown by the controller 102 of Houston or by the combinations of 102 and 114 or 102 and 121. Claim 1 calls for the bus controller to interface with a mass storage device without a mass storage controller as would be the case with HDs of Houston, e.g., see Figure 2, controller 214.

Further, as discussed in the prior amendments, Houston shows a computer architecture that lacks a controller having a memory interface and a mass storage interface. North Bridge element 102, by itself, has only a memory interface and a PCI bus interface, not a mass storage interface. Accordingly, Houston does not show or fairly suggest the invention of claims 17 and 18.

Conclusion

In view of all of the above, it is requested that a timely Notice of Allowance be issued in this case.

No fee is believed due with this Amendment. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

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